Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : STM32WB15 & STM32WB10 - product enhancement

PCN Reference : MDG/22/13164

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STM32WB15CCU6E	STM32WB15CCY6TR	STM32WB10CCU5
STM32WB15CCU7E	STM32WB15CCU7	STM32WB15CCU6

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PRODUCT/PROCESS CHANGE NOTIFICATION
PCN13164 – Additional information

STM32WB15 and STM32BW10 - product enhancement

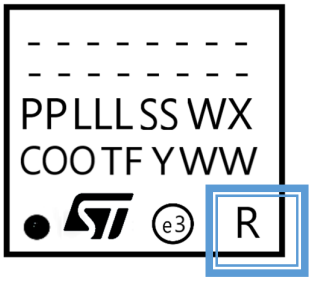
MDG - Microcontrollers Division (MCD)

What are the changes?

Changes described in table below:

STM32WB15/10	Current Cut2.0	New Cut2.1
Die revision Marking **R**	“B”	“Z”

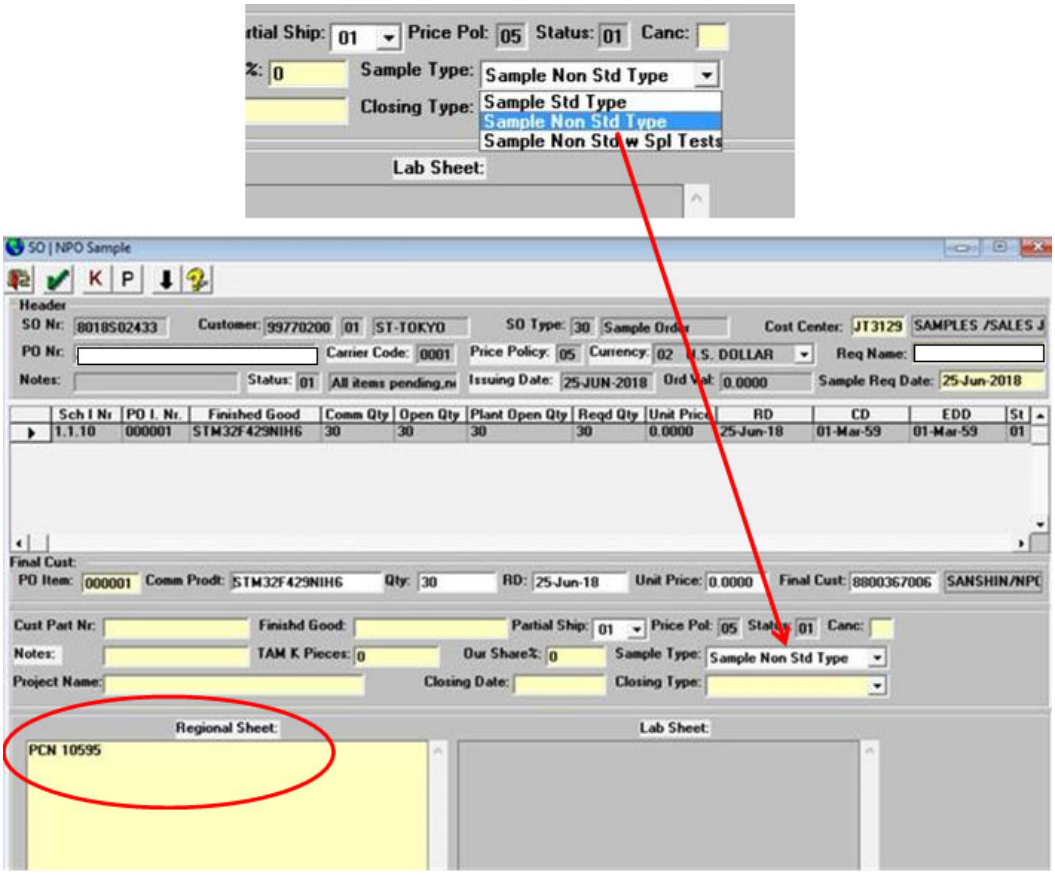
Example: Marking on package UFQFPN 7X7X0.55 48L



How to order samples?

For all samples request linked to this PCN, please:

- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "**PCN13034**" into the NPO Electronic Sheet/**Regional Sheet**
- request sample(s) through Notice tool, indicating a single Commercial Product for each request



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Reliability Evaluation Report

MDG-MCD- RERMCD1914

STM32WB10/15XX (494x66)

Reliability Evaluation Purpose **(New Product Qualification)**

General Information	
Commercial Product	STM32WB10CC/ STM32WB15CC
Product Line	494X66
Die revision	494XXXZ (Cut2.1)
Product Description	STM32WB10/WB15XX family
Package	UFQFPN 7X7X0.55 48L 0.5 MM PITCH, WLCSP 49L P 0.4
Silicon Technology	CMOS 90nm LP RF option
Division	MDG-MCD
Reliability Maturity Level	20->W29

Traceability	
Diffusion Plant	TSMC Fab14, Taiwan.
Assembly Plant	JSCC, China. ATT1/ATT3, Taiwan.

Reliability Assessment	
Pass	☒
Fail	☐
Investigation required	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	27th Jan 2021	Laurent CLARAMOND	MDG-MCD-Q&R Engineer

APPROVED BY:

Function	Location	Name	Date
Version 1.0 Division Q&R Manager	Grenoble	Dominique GALIANO	04th Feb 2021
Version 1.0 Division Quality Manager	Rousset	Pascal NARCHE	10th Feb 2021
Version 1.1 Division Q&R Manager	Grenoble	Dominique GALIANO	09th Feb 2022

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation performed on STM32WB10/15XX Die 494XXXA (Cut 1.0), 494XXXB (Cut 2.0) and 494XXXZ (Cut 2.1).

Test vehicle is described here below:

Product	Process / Package	Diffusion / Assembly plant
STM32WB15CUU6$71	CMOS 90nm LP RF option UFQFPN48 7X7	TSMC Fab14, SC-StatsChippac-China 998Z JSCC/JSCC
STM32WB15CUU6$72	CMOS 90nm LP RF option UFQFPN48 7X7	TSMC Fab14, SC-StatsChippac-China 998Z JSCC/JSCC
STM32WB15CUU6E$71	CMOS 90nm LP RF option UFQFPN48 7X7	TSMC Fab14, SC-StatsChippac-China 998Z JSCC/JSCC
STM32WB15CUU6$73	CMOS 90nm LP RF option UFQFPN48 7X7	TSMC Fab14, SC-StatsChippac-China 998Z JSCC/JSCC
STM32WB15CUY6$T1	CMOS 90nm LP RF option WLCSP 49L	TSMC Fab14, SC AMKOR ATT1/ATT3

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

1.2 Reliability Strategy

The STM32WB10 - 320KB and the STM32WB15 - 320KB (Die 494XXX) are based on STM32L4x product family , the STM32WB55 product (Die 495) and the STM32WB35 product (Die 496), processed in TSMC90nm technology in FAB14

STM32L486x (die 415): RERMCD1112
STM32L433x (die 435): RERMCD1424
STM32L452x (die 462): RERMCD1526
STM32L496x (die 461): RERMCD1521
STM32WB55x (die 495): RERMCD1613
STM32WB35x (die 496): RERMCD1801

The RF option is already qualified via AMG RF products BlueNRG-MS (DM00559663), Reach-1D (DM00559677) and BlueNRG-1(DM00559904) and with the STM32WB55x (RERMCD1613) and with the STM32WB35x (RERMCD1801).

The STM32WB10 - 320KB and the STM32WB15 - 320KB (Die 494XXX) device are assembled in the following package already qualified at Division level:

Package	Reference	Assy Plant location
UFQFPN48 7x7x0.55 P0.5	RERMCD1622 RERMCD1613	JSCC China
WLCSP49L	RERMCD1112 RERMCD1613	Amkor Taiwan ATT1

Based on these data, and according to "RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION" specification (DMS 0061692), the following qualification strategy has been defined:

Die Qualification:

- 1 reliability lot on 494XXXA (Cut 1.0) in UFQFPN48 STM32WB15CUU6$71 from JSCC (China, Jiangyin)
- 1 reliability lot on 494XXXB (Cut 2.0) in UFQFPN48 STM32WB15CUU6$72 from JSCC (China, Jiangyin) for HTOL 168H, ESD HMB and LU.
- 1 reliability lot on 494XXA (cut 1.0) in UFQFPN48 STM32WB15CUU6E$71from JSCC (China, Jiangyin) for HBM, CDM and LU. Same design, SMPS is not connected to the package, while 2 more GPIOs are connected to the package.
- 1 reliability lot on 494XXXZ (Cut 2.1) in UFQFPN48 STM32WB15CUU6$73 from JSCC (China, Jiangyin) for HTOL 168H, ESD HMB and LU.

Package Qualification:

- The reliability test plan and result summary are presented in the following tables:

Package	Body	Pitch	Package Code	Wire	Assembly	Bonding Option	Trial
UFQFPN48	7x7	0.5	AB029	Gold	JSCC	0.8 mil	1 lot for package trials with STM32WB15CUU6$71
UFQFPN48	7x7	0.5	AB029	Gold	JSCC	0.8 mil	1 lot for ESD CDM with STM32WB15CUU6$71 STM32WB15CUU6E$71and STM32WB15CUU6$72
WLCSP49	3.301x 3.375	0.4	B0DE		ATT1		1 lot for ESD CDM with STM32WB15CUY6$T1 (note 1)

Note 1: This WLCSP use same BOM than qualified for die 462 with 6.3um RDL. Die size 11.3mm3 is similar to die 462 (12.5 mm2). Therefore, only CDM is required.

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for STM32WB10 - 320K and STM32WB15 - 320KB - Die 494XXXZ (cut 2.1) assembled in UFQFPN48 7X7 and WLCSP49L 3.301x 3.375.

However, one failure on SMPS leakage test was revealed at HTOL 168h readout on STM32WB55x - 1M-Die 495XXXX (cut2.2) UFQFN 7x7, which is due to parasitic inductance from HTOL chipboard PCB layout on SMPS pins is exceeding what will be limited in product Errata Datasheet.

As Die 494XXXZ (cut 2.1) embed same SMPS IP than Die 495XXXX (cut2.2), a new HTOL exercise on Die 495XXXX (cut2.2) is being launched in the recommended conditions of errata, result will be published in Q3 2022.

Refer to Section 3.2 for reliability test results.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

STM32WB10/15XX (die 494) is derivate from STM32WB55XX (die 495) and STM32WB15XX (die 496) products. The main differences are linked to the decrease of the memories (NVM from 1Mo to 320K & RAM from 256KB to 48KB).

For additional information concerning the product behavior, refer to STM32WB10/WB15XX datasheets.

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information	
FAB1	
Wafer fab name / location	TSMC Fab14 / Taiwan
Wafer diameter (inches)	12
Wafer thickness (µm)	775 +/- 25
Silicon process technology	TSMC090 ULL
Number of masks	48
Die finishing front side (passivation) materials/thicknesses (µm)	PSG + NITRIDE, 1.1
Die area (Stepping die size) (µm)	12.5 mm²
Die pad size (X,Y) (µm)	123x59
Sawing street width (X,Y) (µm)	80, 80
Metal levels/Materials/Thicknesses (µm)	Metal 1 TaN/Ta/CuSeed/Cu 0.240 um Metal 2 TaN/Ta/CuSeed/Cu 0.310 um Metal 3 TaN/Ta/CuSeed/Cu 0.310 um Metal 4 TaN/Ta/CuSeed/Cu 0.310 um Metal 5 TaN/Ta/CuSeed/Cu 0.310 um Metal 6 TaN/Ta/CuSeed/Cu 0.850 um Metal 7 TaN/CuSeed/Cu 3.400 um Metal 8 AlCu 1.450 um
Die over coating (material/thickness)	No
FIT level (Ea=0.7eV, C.L: 60%, 55°C)	3.1 FITs at qualification date.
Soft Error Rate - Alpha SER [FIT/Mb] - Neutron SER [FIT/Mb] - Conditions	Alpha SER: 491 FIT/Mb Neutron SER: 445 FIT/Mb Neutron SER is an estimation at sea level of NYC (14n/h/cm²). Alpha result is estimated using a nominal flux of 0.001α/h/cm²
Wafer Level Reliability - Electro-Migration (EM) - Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) - Hot Carrier Injection (HCI) - Negative Bias Thermal Instability (NBTI) - Stress Migration (SM)	Yes
Other Device(s) using same process	STM32L4x product family, 415, 435, 461, 462 STM32WB55x 495, STM32WB15x 496 product family

2.2.2 Assembly information

Table 2

Assembly Information	
Package 1 - UFQFN48 7X7	
Assembly plant name / location	Statschippac Semi-conductor 998Z Shanghai Co., Ltd. 188 Hua Xu Road Shanghai (China)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 +/- 25µm
Die sawing method	Laser Grooving + Mechanical dicing
Bill of Material elements	
Lead Frame material/reference	Rough Cu LF UQFN48L 5.2sq Groove JSCC
Die attach material/type(glue/film)/supplier	Glue Hitachi EN4900GC
Wire bonding material/diameter/	0.8mils 3N Gold wire
Molding compound material/supplier/reference	EME-G770 Sumitomo
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Assembly Information	
Package 2 - WLCSP49L	
Assembly plant name / location	Amkor Taiwan ATT1, Z6SA AMKOR ATT1 996S
Pitch (mm)	0.4
Die thickness after back-grinding (µm)	380+/-25 µm
Die sawing method	Laser Grooving + Mechanical dicing
Bill of Material elements	
Balls metallurgy/diameter	Solder ball SAC405 Diam 230um
Routing/Redistribution layer (RDL) material	RDL Copper 6um
PBO passivation material /supplier	PBO passivation HD8820
Backside coating material	Back side coating PET film
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 1

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	ST GRAL in Grenoble

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
1	P63V32 Wafer#6	1.0	GQ00927Z	78MI*494ZZXA	UFQFN48 7x7	Die and package Reliability assessment.
2	P63V32 Wafer#19	1.0	GQ0142CM	79MI*494ZZXA	UFQFN48 7x7	ESD HBM, CDM and LU
3	P63V32 Wafer#7	1.0	A5009017	T92Q*494ZZXA	WLCSP49L	ESD CDM
4	P65H03 Wafer#4	2.0	GQ04521N	78MI*494ZZXB	UFQFN48 7x7	HTOL , ESD HBM, CDM and LU
5	P65H04 Wafer#8	2.1	GQ1372AJ	78MI*494ZZXZ	UFQFN48 7x7	HTOL , ESD HBM, CDM and LU

3.2 Test plan and results summary

Table 5 - ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lot#	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Ta 125°C VDD 3V6 Duration 1200h	1	77	77	Lot1: 0/77	*Cut 1.0*
HTOL	JESD22 A108	Ta 125°C VDD 3V6 Duration 168h	2	77	77	Lot4: 0/77 Lot5: 0/77	*Cut 2.0* *Cut 2.1*
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF 2kV class2	4	3	3	Lot1: 0/3 Lot2: 0/3 Lot4: 0/3 Lot5: 0/3	*Cut 1.0* *Cut 1.0* *Cut 2.0* *Cut 2.1*
Latch Up	JESD78	130°C	4	3	3	Lot1: 0/3 Lot2: 0/3 Lot4: 0/3 Lot5: 0/3	*Cut 1.0* *Cut 1.0* *Cut 2.0* *Cut 2.1*
EDR	JESD22-A117	10kcy EW @ 125°C then Storage HTB 150°C - Duration 1500H	1	77	77	Lot1: 0/77	*Cut 1.0*
EDR	JESD22-A117	10kcy EW @ 25°C then Storage HTB 150°C - Duration 168h	1	77	77	Lot1: 0/77	*Cut 1.0*
EDR	JESD22-A117	10kcy EW @ -40°C then Storage HTB 150°C - Duration 168H	1	77	77	Lot1: 0/77	*Cut 1.0*
ELFR	JESD22-A108 JESD74	Ta=125°C Vdd : 3V6 Duration= 48hrs	1	500	500	Lot1: 0/500	*Cut 1.0*

Table 6 - ACCELERATED ENVIRONMENT STRESS TESTS for UFQFN48 7X7

Test code	Stress method	Stress Conditions	Lot#	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot1 0/308	*Cut 1.0*
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot1 0/77	*Cut 1.0*
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot1 0/77	*Cut 1.0*
UHAST	JESD 22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot1 0/77	*Cut 1.0*
THB	JESD 22-A101	Ta=85°C/85%RH Duration= 1000hrs VDD=3v6 ☒ After PC	1	77	77	Lot1 0/77	*Cut 1.0*
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V class2a	4	3	3	Lot1: 0/3 Lot2: 0/3 Lot4: 0/3 Lot5: 0/3	*Cut 1.0* *Cut 1.0* *Cut 2.0* *Cut 2.1*

Table 7 - ACCELERATED ENVIRONMENT STRESS TESTS for WLCSP49L

Test code	Stress method	Stress Conditions	Lot#	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V class2a	3	3	3	Lot3: 0/3	*Cut 1.0*

Note: Test method revision reference is the one active at the date of reliability trial execution

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A110:	Temperature Humidity Bake
JESD 22B102:	Solderability test
JESD22B100/B108:	Physical dimension

5 GLOSSARY

Reference	Short description
HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HAST	Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up
CA	Construction Analysis

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Laurent CLARAMOND	Initial Release	Div. Quality Manager	Rousset	Pascal NARCHE	10th Feb 2021
			Q&R Quality Manager	Grenoble	Dominique GALIANO	04th Feb 2021
1.1	Moses TAN	Updated with cut2.1 results	Q&R Quality Manager	Grenoble	Dominique GALIANO	09th Feb 2022

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